AMENDMENTS TO THE CLAIMS:

Claim 1. (Currently amended) A method of forming a semiconductor device, comprising:

lithographically patterning ~~providing~~ a structure having a first critical dimension~~; forming a lithographic pattern~~, wherein said structure includes nested features and an isolated feature ~~on said structure~~;

etching said structure with an O2-containing material to trim said first critical dimension to a second critical dimension to correct~~, said second critical dimension being smaller than said first critical dimension; and~~

~~correcting~~ an offset between a said nested features ~~feature printed on said structure~~ and said ~~an~~ isolated feature created by said lithographic patterning ~~printed on said structure~~.

Claim 2. (Canceled)

Claim 3. (Currently amended) The method of claim 1, further comprising:

forming a positive photoresist layer over a substrate ~~said structure~~ prior to forming said ~~lithographic pattern on said~~ structure in said photoresist layer.

Claim 4. (Currently amended) The method of claim 1 2, wherein said ~~correcting includes:~~

~~forming~~ structure comprises a negative photoresist ~~over said nested feature and said isolated feature~~; and

wherein said etching comprises ~~said semiconductor substrate using~~ a surface charging technique in combination with a plasma etch, such that said nested feature is etched faster than said isolated feature.

Claim 5. (Original) The method of claim 1, wherein said second critical dimension is within a range of about 10-50 nm smaller than said first critical dimension.

Claim 6. (Original) The method of claim 1, wherein said etching is performed at approximately 5mT to approximately 50mT for a time of between approximately 5 seconds to approximately 40 seconds.

B1 cont.

Claim 7. (Original) The method of claim 1, wherein said structure includes an anti-reflection coating formed on a polysilicon substrate.

Claim 8. (Currently amended) A method of trimming a structure ~~conductor~~ on a substrate, comprising:

lithographically patterning ~~providing~~ a structure ~~conductor~~ having a first critical dimension, wherein said structure includes nested features and an isolated feature ;

~~forming a lithographic pattern on said conductor;~~

etching said structure ~~conductor~~ with an O2-containing material to trim said first critical dimension to a second critical dimension, said second critical dimension being smaller than said first critical dimension to correct; ~~and~~

~~correcting~~ an offset between said a nested features ~~feature printed on said structure~~ and said ~~an~~ isolated feature ~~printed on said structure~~.

Claim 9. (Canceled)

Claim 10. (Currently amended) The method of claim 8, wherein said structure comprises ~~further comprising: forming~~ a positive photoresist ~~over said conductor prior to forming said lithographic pattern on said conductor~~.

Claim 11. (Original) The method of claim 8, wherein said second critical dimension is within a range of about 10-50 nm smaller than said first critical dimension.

B1 cont.

Claim 12. (Original) The method of claim 8, wherein said etching is performed at approximately 5mT to approximately 50mT for a time of between approximately 5 seconds to approximately 40 seconds.

Claim 13. (Currently amended) The method of claim 8, wherein said structure ~~conductor~~ includes a polysilicon substrate having an anti-reflection coating formed thereon.

Claim 14. (Original) A method of etching a semiconductor device, comprising:

lithographically forming nested features and an isolated feature; and

etching said semiconductor device using a surface charging technique in combination with a plasma etch, such that a nested features ~~feature~~ formed on said semiconductor device are ~~is~~ etched faster than an isolated feature formed on said semiconductor device to compensate for an offset between said nested features and said isolated features which resulted from said lithographic formation of said nested features and said isolated features.

Claim 15. (Canceled)

Claim 16. (Currently amended) The method of claim 14, wherein said nested features and said isolated feature comprise a negative photoresist ~~is provided over said nested feature and said isolated feature~~.

B1 cont.

Claim 17. (Original) The method of claim 14, wherein said etching uses a mixture of NF3 and argon.

Claim 18. (Original) The method of claim 14, wherein said semiconductor device includes a polysilicon substrate, a TEOS layer formed over the substrate, and an antireflection coating layer formed over the substrate.

Claim 19. (Currently amended) A method of etching a semiconductor material, comprising:

lithographically forming ~~providing a semiconductor substrate including a~~ nested features ~~feature~~ and an isolated feature~~; forming~~, wherein said nested features and said isolated feature comprises a negative photoresist ~~over said nested feature and said isolated feature~~; and

etching said semiconductor substrate using a surface charging technique in combination with a plasma etch, such that said nested feature is etched faster than said isolated feature to compensate for an offset between said nested features and said isolated feature created by said lithographic forming.

B1 cont.

Claim 20. (Currently amended) The method of claim 19, wherein said features are formed on a semiconductor substrate which comprises ~~includes~~ a polysilicon substrate, and wherein said nested features and said isolated feature comprise a TEOS layer and an antireflection coating layer ~~are formed over the substrate~~.